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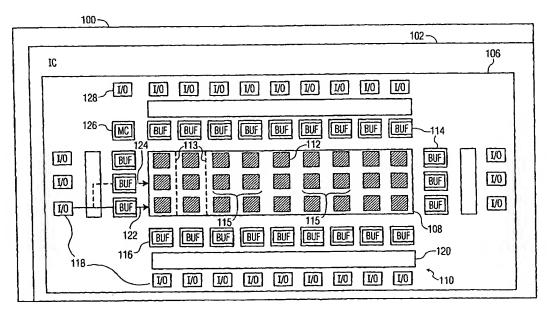
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[Continued on next page]

(54) Title: MODULAR INTEGRATION OF AN ARRAY PROCESSOR WITHIN A SYSTEM ON CHIP



(57) Abstract: A systolic array processor is integrated within a system on chip (SoC) in a format that is compatible with existing and emerging SoC technologies. The systolic array processor may be implemented as a co-processor to a general-purpose digital signal processor or as a functional unit of a very long instruction word (VLIW) processor.

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.



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A. CLASSIFICATION OF SUBJECT MATTER IPC 7 G06F15/76 G06F9/38								
According to	According to International Patent Classification (IPC) or to both national classification and IPC							
B. FIELDS								
Minimum documentation searched (classification system followed by classification symbols) IPC 7 G06F								
Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched								
Electronic data base consulted during the International search (name of data base and, where practical, search terms used) EPO-Internal, INSPEC								
C. DOCUME	ENTS CONSIDERED TO BE RELEVANT							
Category °	Citation of document, with indication, where appropriate, of the r	relevant passages	Relevant to claim No.					
Y	MIYAMORI T ET AL: "REMARC: RECOMULTIMEDIA ARRAY COPROCESSOR" IEICE TRANSACTIONS ON INFORMATION SYSTEMS, INSTITUTE OF ELECTRONIC INFORMATION AND COMM. ENG. TOKYOVOI. E82-D, no. 2, February 1999 (1999-02), pages XP000821922 ISSN: 0916-8532 the whole document	ON AND CS O, JP,	1-20					
X Furt	ther documents are listed in the continuation of box C.	X Patent family	members are listed in annex.					
° Special co 'A' docum consist 'E' earlier	ategories of cited documents: ent defining the general state of the art which is not dered to be of particular relevance document but published on or after the international	"T" later document proof or priority date a cited to understainvention "X" document of parti	"T" later document published after the International filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention "X" document of particular relevance; the claimed invention					
which citatio	ent which may throw doubts on priority claim(s) or its cited to establish the publication date of another on or other special reason (as specified) more affairing to an oral disclosure, use, exhibition or a property of the international filing date but	involve an inven "Y" document of particannot be consided comment is corments, such corin the art.						
4	actual completion of the international search		24 document member of the same patent family Date of mailing of the international search report					
	23 December 2004		30/12/2004					
Name and	mailing address of the ISA European Patent Office, P.B. 5818 Patentlaan 2 Nt 2280 HV Rijswijk		Authorized officer					
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	ation) DOCUMENTS CONSIDERED TO BE RELEVANT Citation of document, with indication, where appropriate, of the relevant passages	Relevant to daim No.
category °	Citation of document, with indication, where appropriate, or the relevant passages	
r	CUCCHIARA R ET AL: "RECONFIGURING THE BOUNDARIES OF A MESH-CONNECTED ARRAY OF PROCESSORS WITH RUN-TIME PROGRAMMABLE LOGIC" MICROPROCESSORS AND MICROSYSTEMS, IPC BUSINESS PRESS LTD. LONDON, GB, vol. 17, no. 2, January 1993 (1993-01), pages 67-73, XP000355541 ISSN: 0141-9331 page 68, left-hand column, line 37 - line 69 page 69, right-hand column, line 22 - line 32; figure 1	1-20
X	BARAT F ET AL INSTITUTE OF ELECTRICAL AND ELECTRONICS ENGINEERS: "Reconfigurable instruction set processors: an implementation platform for interactive multimedia applications" CONFERENCE RECORD OF THE 35TH. ASILOMAR CONFERENCE ON SIGNALS, SYSTEMS, & COMPUTERS. PACIFIC GROOVE, CA, NOV. 4 - 7, 2001, ASILOMAR CONFERENCE ON SIGNALS, SYSTEMS AND COMPUTERS, NEW YORK, NY: IEEE, US, vol. VOL. 1 OF 2. CONF. 35, 4 November 2001 (2001-11-04), pages 481-485, XP010580968 ISBN: 0-7803-7147-X page 482, paragraph 2 - page 484	13-19
X	CALLAHAN T J ET AL: "THE GARP ARCHITECTURE AND C COMPILER" COMPUTER, IEEE COMPUTER SOCIETY, LONG BEACH., CA, US, US, vol. 33, no. 4, April 2000 (2000-04), pages 62-69, XP000948675	1,6,7,20
А	ISSN: 0018-9162 the whole document	13
А	SINGH H ET AL: "MorphoSys: a reconfigurable architecture for multimedia applications" INTEGRATED CIRCUIT DESIGN, 1998. PROCEEDINGS. XI BRAZILIAN SYMPOSIUM ON RIO DE JANEIRO, BRAZIL 30 SEPT3 OCT. 1998, LOS ALAMITOS, CA, USA, IEEE COMPUT. SOC, US, 30 September 1998 (1998-09-30), pages 134-139, XP010303762 ISBN: 0-8186-8704-5 the whole document	
1		



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PCT/IB 03/05625

	INTERNATIONAL GENERALITATION	101718 03/03020
C.(Continua	tion) DOCUMENTS CONSIDERED TO BE RELEVANT Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
Category °	Citation of document, with indication, where appropriate, or the rest and passage	
A	YATES R B ET AL: "AN ARRAY PROCESSOR FOR GENERAL PURPOSE DIGITAL IMAGE COMPRESSION" IEEE JOURNAL OF SOLID-STATE CIRCUITS, IEEE INC. NEW YORK, US, vol. 30, no. 3, 1 March 1995 (1995-03-01), pages 244-249, XP000502810 ISSN: 0018-9200 the whole document	1-20
A	WO 94/06077 A (SIEMENS AG ; BUCHENRIEDER KLAUS (DE)) 17 March 1994 (1994-03-17) the whole document	1-20
А	PRADO E R ET AL: "A high performance COTS based vector processor for space" MAPLD CONFERENCE, XX, XX, 28 September 1999 (1999-09-28), pages 1-6, XP002207357 the whole document	1,11-13,
	·	
97		



Inter nal A no n No PCT/IB 03/05625

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
WO 9406077 A	17-03-1994	WO 9406077 A1 DE 59301609 D1 DK 657044 T3 EP 0657044 A1 ES 2083296 T3	17-03-1994 21-03-1996 25-03-1996 14-06-1995 01-04-1996